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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,677	02/18/2004	Dae-Seung Jeong	9862-000017/US	8542

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EXAMINER	
TIMORY, KABIR A	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/779,677	JEONG ET AL.	
	Examiner	Art Unit	
	KABIR A. TIMORY	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments filed on 01/04/2008, with respect to finality of the last office action have been fully considered and are persuasive. Therefore, finality of the last office action has been withdrawn.

2. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-17 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izzard et al (US 5,506,874) in view of Rogers et al. (IEEE Journal of Solid-State Circuits. VOL.37, NO. 12, DECEMBER 2002).

Regarding claim 1:

As shown in figure 1-11, Izzard et al discloses a quarter-rate phase detector comprising:

- an error circuit (20, 22 in figure 1) to combine corresponding ones of the latched signals respectively, resulting in a plurality of intermediate signals (column 1, lines 36-39); and
- a multiplexing unit(24 in figure 1) to selectively output the intermediate signals as a phase error signal (PI in figure 1).

Izzard et al. discloses all of the subject matter as described above and four latches except for specifically teaching four latches controllable to latch, at different times according to quadrature clock signals respectively, data received by the phase detector (figure 9, 10) so as to form latched signals.

However, Rogers et al. in the same field of endeavor, teaches four latches controllable to latch, at different times according to quadrature clock signals respectively, data received by the phase detector so as to form latched signals (figure 4).

One of ordinary skill in the art would have clearly recognized that a phase detector is a frequency mixer or analog multiplier circuit that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the phase-locked loop (PLL). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a quarature phase detector which contains four latches as taught by Rogers et al. in the method and system of Izzard et al. in order to phase error signal.

Regarding claim 2:

Izzard et al. discloses all of the subject matter as described above except for specifically teaching wherein:

- the quadrature clock signals include signals I, Q, Ib and Qb;
- a flrst one of the latches is controlled by I;
- a second one of the latches is controlled by Q;
- a third one of the latches controlled by Ib; and
- a fourth one of the latches is controlled by Qb.

However, Rogers et al. in the same field of endeavor, teaches wherein:

- the quadrature clock signals include signals I, Q, Ib and Qb 9 figure 4);
- a first one of the latches is controlled by I (CI in figure 4);
- a second one of the latches is controlled by Q (CQ in figure 4);
- a third one of the latches controlled by Ib (CI 'bar" in figure 4); and
- a fourth one of the latches is controlled by Qb (CQ "bar" in figure 4).

One of ordinary skill in the art would have clearly recognized that a phase detector is a frequency mixer or analog multiplier circuit that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the phase-locked loop (PLL). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a quarature phase detector which contains four latches as taught by Rogers et al. in the method and system of Izzard et al. in order to phase error signal.

Regarding claim 3:

Izzard et al. further discloses wherein:

- the multiplexing unit is controllable by the quadrature clock signals (figure 9, 24).

Regarding claim 4:

Izzard et al. further discloses wherein the multiplexing unit is controllable to truncate the intermediate signals (figure 1, MI' and MI").

Regarding claim 5:

Izzard et al. further discloses wherein:

- the multiplexing unit is operable to form the phase error signal by cycling through the truncated intermediate signals (figure 1, MI' and MI", column 3, lines 5-19).

Regarding claim 6:

Izzard et al. further discloses wherein:

- the quadrature clock signals include signals I and Q; and the multiplexing unit is controlled according to the signals I and Q, respectively (figure 1, MI' and MI", column 3, lines 5-19).

Regarding claim 7:

Izzard et al. further discloses wherein the multiplexing unit includes:

- a first multiplexer and a second multiplexer to receive the intermediate signals, respectively (figure 9, 28, 32); and
- a third multiplexer to multiplex outputs of the first and second multiplexers (figure 9, 24).

Regarding claim 8:

Izzard et al. further discloses wherein

- the corresponding latched signals are pairs of latched signals (figure 9 MI' and MI"); and
- each pair has a first set and a second set, the second set representing the latched signals subsequently closest in time to the first set, respectively (figure 9 MI' and MI", column 3, lines 14-19).

Regarding claim 9:

Izzard et al. further discloses wherein:

- the error circuit includes four exclusive OR (XOR) gates, each XOR gate receiving one of the pairs, respectively (figure 9, 20, 22, 26, 30).

Regarding claim 10:

Izzard et al. further discloses wherein:

- the four latches represent a first set of latches and the latched signals represent a first set of latched signals (figure 9, 12a, 12b, 16a, 16b, MI');

the detector further comprises:

- a second set of four latches arranged to receive the outputs of the first set of latches (figure 9, 14a, 14b, 18a, 18b), respectively, and controllable to latch data at different times according to the quadrature clock signals, respectively, so as to form a second set of latched signals (column 2, lines 43-48); and
- the second set representing re-timed versions of the received data (signals being output from second set of latches 14a, 14b, 18a, 18b, are interpreted to be the re-timed version of the received data) (figure 9).

Regarding claim 11:

Izzard et al. further discloses wherein:

- the second set of latched signals is organized as pairs (figure 9, 14a, 14b, 18a, 18b); the detector further comprises:
- a reference circuit to generate a reference signal based upon transitions in the second set of latched signals (figure 9, MI").

Regarding claim 12:

Izzard et al. further discloses wherein:

- the second set of latched signals is organized as pairs (figure 9, 14a, 14b, 18a, 18b); the reference circuit includes:
- a plurality of multiplexers to selectively output the pairs of re-timed data (signals being output from second set of latches 14a, 14b, 18a, 18b, are interpreted to be the re-timed version of the received data) (figure 6, 24a, 24b);
- and an exclusive OR (XOR) gate to receive the outputs of the plurality of multiplexers (figure 6, 24a, 24b, 20).

Regarding claim 13:

Izzard et al. further discloses wherein:

- the rate of the intermediate signals is 1/4 of the received data rate (column 5, lines 31-32).

Regarding claim 14:

As shown in figure 1-11, Izzard et al discloses a quarter-rate phase detector comprising:

- four data latches, each latch receiving the same input data (figure 9, 12a, 12b, 16a, 16b, D), respectively, so as to produce latched signals (figure 9); and
- an error signal-generating circuit to generate a phase error signal based upon the four latched signals and the quadrature clocks signals (figure 9, MI').

Izzard et al. discloses all of the subject matter as described above and four latches except for specifically teaching the latches being clocked by quadrature clock signals.

However, Rogers et al. in the same field of endeavor, teaches the latches being clocked by quadrature clock signals (figure 4).

One of ordinary skill in the art would have clearly recognized that a phase detector is a frequency mixer or analog multiplier circuit that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the phase-locked loop (PLL). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a quarature phase detector which contains four latches as taught by Rogers et al. in the method and system of Izzard et al. in order to phase error signal.

Regarding claim 15:

Izzard et al. further discloses wherein

- the error-signal-generating circuit is operable upon the four latched signals and is controlled by the quadrature clocks signals (figure 9, MI', column 2, lines 43-45).

Regarding claim 16:

As shown in figure 1-11, Izzard et al discloses a quarter-rate phase detector comprising:

- four XOR gates receiving latched signals (figure 9, 20, 22, 26, 30), respectively, each XOR gate generating an intermediate signal (figure 9, MI' and MI");
- a multiplexer to selectively output one of the four intermediate signals as a phase error signal (figure 9, 24).

Izzard et al. discloses all of the subject matter as described above and four latches except for specifically teaching each latched signal corresponding to input data latched according to one of quadrature clock signals.

However, Rogers et al. in the same field of endeavor, teaches each latched signal corresponding to input data latched according to one of quadrature clock signals (figure 4).

One of ordinary skill in the art would have clearly recognized that a phase detector is a frequency mixer or analog multiplier circuit that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the phase-locked loop (PLL). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a quarature phase detector which contains four latches as taught by Rogers et al. in the method and system of Izzard et al. in order to phase error signal.

Regarding claim 17:

Izzard et al. further discloses:

- four data latches, each latch receiving the same input data (figure 9, D), the latches being clocked by quadrature clock signals (column 2, lines 43-45), respectively, so as to produce quadrature latched data signals (column 2, lines 43-45).

Regarding claim 21:

As shown in figure 1-11, Izzard et al discloses a method of detecting phase at a quarter of the rate of the received data, the method comprising:

- combining corresponding ones of the latched signals, respectively, to provide a plurality of intermediate signals (figure 9, MI' & MI"); and
- selectively outputting one among the intermediate signals, respectively, to provide a constructed a phase error signal (figure 9, 24).

Izzard et al. discloses all of the subject matter as described above and four latches except for specifically teaching latching, at different times according to quadrature clock signals, respectively, the received data so as to form latched signals.

However, Rogers et al. in the same field of endeavor, teaches latching, at different times according to quadrature clock signals, respectively, the received data so as to form latched signals (figure 4).

One of ordinary skill in the art would have clearly recognized that a phase detector is a frequency mixer or analog multiplier circuit that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the phase-locked loop (PLL). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a quarature phase

detector which contains four latches as taught by Rogers et al. in the method and system of Izzard et al. in order to phase error signal.

Regarding claim 22:

Izzard et al. further discloses wherein:

- the quadrature clock signals include signals I and Q; and the selectively outputting step selectively outputs according to the signals I and Q, respectively (column 2, lines 43-48).

Regarding claim 23:

Izzard et al. further discloses wherein:

- the rate of the quadrature clock signals is 1/4 of the received data rate (column 5, lines 31-32).

5. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izzard et al. in view of Savoj et al. (US 6,847,789).

Regarding claim 18:

As shown in figure 11, Izzard et al discloses a clock and data recovery (CDR) circuit comprising:

- a phase-error generating circuit to determine quarter-rate phase detector(figure 11, 10, column 2, lines 43-45);
- a filter operable upon an output of the charge pump; and

- a quadrature voltage-controlled oscillator (VCO) operable upon an output of the filter;
- the phase-detector being controllable by the output of the VCO.

Izzard et al discloses all of the subject matter as described above except for specifically teaching a charge pump operable upon an output of the phase detector.

However Savoj et al. in the same field of endeavor, teaches a charge pump operable upon an output of the phase detector (figure 2, 220,).

One of ordinary skill in the art would have clearly recognized that a phase lock loop (PLL) and clock and data recovery (CDR) circuit are generally include a phase detector to generate a voltage signal which represents the difference in phase between two signal input, a charge pump to generate either higher or lower voltage power source for the LPF and VCO using capacitors as storage elements, a low-pass filter (LPF) to attenuate frequencies that are higher than the cutoff frequency, and a voltage controlled oscillator (VCO) to be controlled in oscillation frequency oscillation by a voltage input. To generate the desired voltage power, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a charge pump when designing a (PLL) and (CDR) circuits as taught by Savoj et al. Including a charge pump in the CDR circuit would facilitate the operation of PLL and CDR circuit by providing the higher voltage from a low voltage inputs.

Regarding claim 19:

Izzard et al. further discloses, the CDR circuit of claim 18, wherein:

- the rate of the quadrature signals of VCO is 1/4 of the received data rate of the phase-error generating circuit (column 5, lines 31-32).

6. Claim 20 IS rejected under 35 U.S.C. 103(a) as being unpatentable over Izzard et al. in view of Savoj et al. (US 6,847,789) as applied to claim 18 and further in view of Rogers et al.

Regarding claim 20:

Izzard et al. further discloses, the CDR circuit of claim 18, wherein

- the phase-error-generating circuit includes:
- an error circuit to combine corresponding ones of the latched signals respectively (figure 9, MI'), the error circuit providing a plurality of intermediate signals (figure 9, MI' & MI"); and
- a multiplexing unit to selectively output the intermediate signals as a phase error signal (figure 9, 24).

Izzard et al. and Savoj et al. disclose all of the subject matter as described above except for specifically teaching latching four latches controllable to latch, at different times according to quadrature clock signals, respectively, data received by the phase detector so as to form latched signals.

However, Rogers et al. in the same field of endeavor, teaches four latches controllable to latch, at different times according to quadrature clock signals,

respectively, data received by the phase detector so as to form latched signals (figure 4).

One of ordinary skill in the art would have clearly recognized that a phase detector is a frequency mixer or analog multiplier circuit that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the phase-locked loop (PLL). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to use a quarature phase detector which contains four latches as taught by Rogers et al. in the method and system of Izzard et al. in order to phase error signal.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KABIR A. TIMORY whose telephone number is (571)270-1674. The examiner can normally be reached on 6:30 AM - 3:00 PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kabir A Timory/
Examiner, Art Unit 2611
/Shuwang Liu/
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